REMARKS

This Amendment is submitted in response to the Office Action dated June 16, 2005, having a shortened statutory period set to expire September 16, 2005. Proposed amendments to the Claims include amending Claims 1, 4 and 7, canceling Claims 3, 5, 6 and 8-31, and adding Claims 32-35. Upon entry of the proposed amendments, Claims 1, 2, 4, 7 and 32-35 will now be pending.

REJECTIONS UNDER 35 U.S.C. § 102

In paragraph 1 of the present Office Action, the Examiner has rejected Claims 1-31 under 35 U.S.C. 102(e) as being anticipated by Tawil et al. (U.S. Patent Publication No. 2002/0103913 A1 – "*Tawil*"). Applicants respectfully traverse these rejections as applied to the presently pending claims.

Tawil teaches a method and system that permits a host bus adapter to control which target devices are allowed to log in to a port by using an address mask (*Tawil*, Abstract.)

New Claims

With reference now to newly added Claim 32 (which is supported, *inter alia*, by Figure 1 and Figure 2 of the present specification), the cited art does not teach or suggest "a backplane in the computer housing, wherein the backplane includes means for providing an address used to store data in a disk drive; a multiplexer coupled to the disk drive, wherein the multiplexer sends addresses from the backplane and data from a serial data bus that is controlled by an Enclosure Service Interface (ESI) processor; and a Serializer/Deserializer (SER/DES) interposed between the serial data bus and the multiplexer, wherein the SER/DES converts serial data into parallel data to be sent to the disk drive via the multiplexer." *Tawil* generally teaches a system for interconnecting nodes, but does not teach or suggest the specifically claimed features, including a multiplexer that "selectively sends data addresses from the backplane and data from a serial data bus that is controlled by an Enclosure Service Interface (ESI) processor."

With reference to new Claim 33 (which is supported, *inter alia*, on page 6 of the present specification), the cited art does not teach or suggest a system in which "the ESI processor identifies the disk drive from an array of disk drives as being a target disk drive for received or requested data."

With reference to new Claim 34 (which is supported, *inter alia*, at paragraph [0040] of the present specification), the cited art does not teach or suggest that the "serial data bus includes...a separate interrupt line for each disk drive in a plurality of disk drives."

With reference to new Claim 35 (which is supported, *inter alia*, by Figure 3 of the present specification), the cited art does not teach or suggest a method that includes the steps of "during a normal operating state, obtaining, from a backplane in a computer housing, a Fibre Channel Arbitrated Loop (FC-AL) address for data storable in a disk drive; in response to a request for Enclosure Service Interface (ESI) services, switching a multiplexer, which is coupled to the disk drive, to receive data associated with the FC-AL address, wherein the data has been converted from serial form, when on a serial data bus, to parallel form by a Serializer/Deserializer (SER/DES) that is interposed between the multiplexer and the serial data bus; sending the parallel data to the disk drive via the multiplexer; and in response to the parallel data being sent to the disk drive, automatically resetting the multiplexer such that FC-AL addresses can once again be sent from the backplane to the disk drive."

Amended Claims

Reference is now made to Claim 1. Claim 1 is presently amended to include the features of, *inter alia*, now cancelled Claim 3 ("the serial data bus is arranged to operate with an I2C serial protocol"), now cancelled Claim 5 ("the serial data bus is a three line serial data bus"), and now cancelled Claim 6 ("a discrete interrupt connection between the adapter and the enclosure services processor"). Claim 1 also includes the feature of the three line serial data bus "having a data line, a clock line, and an interrupt line," as supported in Figures 1 and 2 of the present specification.

In paragraph 3 of the present Office Action, the Examiner cites paragraph [0004] of *Tawil* against Claim 3 for teaching "that the serial data bus is arranged to operate with an I2C serial protocol." The cited passage relates to the user of a Fibre Channel serial network used to connect nodes, including storage subsystems. While no mention is made of an I2C protocol, the examiner states parenthetically that I2C "is common in conventional computer systems." Applicants respectfully traverse this assumption in light of the present use/environment of the I2C protocol. That is, while I2C is known as a type of bus used to connect integrated circuits (and thus the name Inter-IC), the prior art does not teach or suggest using this protocol in a data bus connected to disk drives. If the Examiner is asserting that this is known as "common knowledge," then Applicants traverse this assertion, and respectfully request adequate evidence of such teaching as required by *MPEP § 2144.04*.

In paragraph 6 of the present Office Action, the Examiner cites paragraph [0004] of *Tawil* against Claim 6 for teaching that the serial data bus comprises "a discrete interrupt connection between the adapter and the enclosure services processor." Applicants respectfully traverse, since the cited art and particularly the cited passage, does not teach or suggest this feature.

In paragraph 6 of the present Office Action, the Examiner cites Newton's telecom dictionary for the definition that a bus is "two or more line", and applies this definition against Claim 5 for teaching that "the serial data bus is a three line serial data bus." However, the cited art does not teach or suggest that these three lines include "a data line, a clock line, and an interrupt line."

CONCLUSION

As the cited prior art does not teach or suggest all of the limitations of the pending claims, Applicants now respectfully request a Notice of Allowance for all pending claims.

No extension of time for this response is believed to be necessary. However, in the event an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time as well as any other fee necessary to further the prosecution of this application to **IBM CORPORATION DEPOSIT ACCOUNT No. 09-0466.**

Respectfully submitted,

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